Masterclock®

Multi-functional Master Clocks

MCR-TCR Module

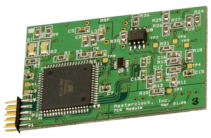
Key Features

- Reads and synchronizes to SMPTE & IRIG time codes
- Software controlled
- Optional Advanced Time Reader (see below)
- Autodetection and automatic gain control of incoming time code
- May be added to **MCR1000**, **MCR5000** or **MCRPCIe**

Additional Option MCR-TCRA

Advanced Time Code Reader Firmware Option

Decode IRIG-A and IRIG-E waveforms



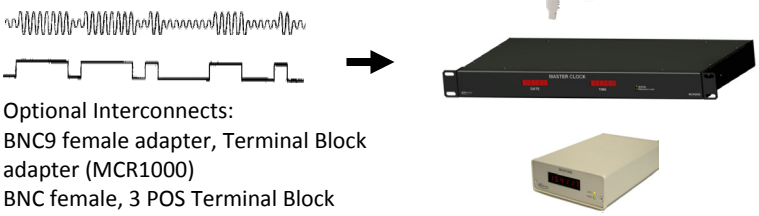
Masterclock's MCR-TCR (Time Code Reader) is an add-in module option for Master Clock Reference devices which reads and synchronizes to SMPTE or IRIG-B time code.

Affordable price and flexible order options make this a popular add-in for synchronizing to time code in broadcast, industry, power distribution and monitoring as well as for specialized military applications.

The TCR option automatically detects and locks to the incoming time code using an automatic gain control circuit. It is software controlled and locks to the most accurate time reference.

Advanced time code reader is an optional feature that enables the decoding of IRIG-A and IRIG-E waveforms.

Each MCR may be ordered with an MCR-TCR module option.



Optional Interconnects:
BNC9 female adapter, Terminal Block adapter (MCR1000)
BNC female, 3 POS Terminal Block (MCR5000, MCRPCIe)

Specifications		Time Codes Read			Additional Time Codes with Advanced TCR Option			
Format		**SMPTE 12M**	**IRIG-B DCLS**	**IRIG-B AM**	**IRIG-A DCLS**	**IRIG-A AM**	**IRIG-E AM**	**IRIG-E DCLS**
Rate		24,25, 30 fps NDF	1kHz, 1mS	1kHz, 1mS	10kHz, 0.1mS	10kHz, 0.1mS	100Hz, 10mS	100Hz, 10ms
Input Level Range		0.2 – 18Vpp 2 Vpp $_{nom}$	0.5 - 12 Vp 5Vp $_{nom}$	0.5 – 8 Vpp 5 Vpp $_{nom}$	0.5 - 12 Vp 5Vp $_{nom}$	0.5 – 8 Vpp 5 Vpp $_{nom}$	0.5 - 12 Vp 5Vp $_{nom}$	0.5 – 8 Vpp 5 Vpp $_{nom}$
Input Impedance kΩ		>10 kΩ			>10 kΩ		>10 kΩ	
Mark to Space Ratio		NA	NA	3.3:1	NA	3.3:1	NA	3.3:1
Automatic Gain Adjust		Over input level range			Over input level range		Over input level range	
Number of Inputs SE: Single Ended - Unbalanced Differential- Balanced		1SE 1DIFF	1SE 1DIFF	1SE 1DIFF	1SE 1DIFF	1SE 1DIFF	1SE 1DIFF	1SE 1DIFF
Type		NDF	DCLS	AM 1kHz	DCLS	AM 10kHz	DCLS	AM 100Hz
ENCODING		None, Leitch Date, SMPTE 309M	None, IEEE 1344 year, IRIG STD 200-04		None, IEEE 1344 year, IRIG STD 200-04		None, IEEE 1344 year, IRIG STD 200-04	
IRIG Coded Expression IRIG STD 200-04	**0 BCD_{TOY}, CF,SBS**	NA	B000	B120	A000	A130	E000	E110
	1 BCD_{TOY}, CF	NA	B001	B121	A001	A131	E001	E111
	2 BCD_{TOY}	NA	B002	B122	A002	A132	E002	E112
	3 BCD_{TOY},SBS	NA	B003	B123	A003	A133	E003	E113
	4 BCD_{TOY}, BCD_{Year}, CF,SBS (IEEE-1344 – 1995 encoding)	NA	B004	B124	A004	A134	E004	E114
	5 BCD_{TOY}, BCD_{Year}, CF	NA	B005	B125	A005	A135	E005	E115
	6 BCD_{TOY}, BCD_{Year},	NA	B006	B126	A006	A136	E006	E116
	7 BCD_{TOY}, BCD_{Year}, SBS	NA	B007	B127	A007	A137	E007	E117

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